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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,643	09/05/2000	Pak Shing Chau	RA-194	7634

7590 05/09/2005

Mark A Lauer
7041 Koll Center Parkway
Suite 280
Pleasanton, CA 94566

EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,643	CHAU ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*, 4/29/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 2/3/05 in which claims 1-23 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura et al U.S. Patent No 6,707,727 B2.

As per claims 1, 12 and 20, Tamura et al teaches a communication system comprising: a first printed circuit board (see figs. 2, 29, 72 and col.1, lines 48-50 and col.38, lines 3-10); a conductive path (see figs. 2, 29, 72 elements 3, 2102, 4020) affixed to the printed circuit board; a driver circuit (see figs. 2, 29, 72 elements 1, 4, 2101, 4010) affixed to the first printed circuit board and coupled to the conductive path to output onto the conductive path a signal having a voltage level that varies time between at least three distinct levels representative of at least three distinct digital values (see col.2, lines 28-65 and col.4, lines 15-18), the driver circuit including an equalization circuit (see fig.72 element 4063 and col.2, lines 65-67 and col.3, lines 28-30 and col.13, lines 19-20 and col.18, lines 5-10 and col.36, lines 5-36) to adjust the voltage level of the signal output by the driver circuit at a first time according to a digital

value represented by the signal at a previous time; and a receiver (see figs. 2, 29, 72 elements 2, 2103, 4060 and col.5, lines 65-67 and col.10, lines 13-14) circuit affixed to the first printed circuit board and coupled to receive the signal from the conductive path to determine which of the at least three distinct digital values is represented by the signal at a given time.

As per claim 2, Tamura et al includes wherein the driver and receiver circuits are respective integrated circuits affixed to the first printed circuit board (see col.38, lines 3-10).

As per claim 3, Tamura et al includes wherein the driver and receiver circuits and conductive path are incorporated within a common integrated circuit that is affixed to the first printed circuit board (see col.38, lines 3-10).

As per claim 4, Tamura et al inherently includes wherein at least one of the driver and receiver circuits is coupled to a second printed circuit board that is affixed to the first printed circuit board.

As per claim 5, Tamura et al inherently includes wherein the second printed circuit board is removably affixed to the first printed circuit board.

As per claim 6, Tamura et al includes wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and delays said plurality of input signals (see figs.4, 12, 13, 15, 16).

As per claim 7, Tamura et al includes wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and inverts said plurality of input signals (see figs.4, 12, 13, 15, 16).

As per claim 8, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for attenuation of the signal in the conductive path.

As per claim 9, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for reflection of the signal in the conductive path.

As per claim 10, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for crosstalk generated by the signal in a second conductive path.

As per claim 11, Tamura et al inherently includes wherein said signal has a fourth voltage level that varies in time between at least three distinct levels, the fourth level representative of a fourth digital value that is distinct from the at least three distinct digital values.

As per claim 13, Tamura et al inherently includes wherein for each of said signal levels, an activation level of said main driver and an activation level of said auxiliary driver sum to equal N.

As per claim 14, Tamura et al inherently includes, wherein said equalization mechanism includes an element adapted to invert said input signals.

As per claim 15, Tamura et al inherently includes wherein said equalization mechanism includes an element adapted to delay said input signals by a time substantially equal to a bit period.

As per claim 16, Tamura et al inherently includes wherein said main driver and said auxiliary driver each include a current source, and said signal levels are voltages that are a range between ground and a positive voltage.

As per claim 17, Tamura et al inherently includes wherein said equalization mechanism is configured to compensate for attenuation of said signal over a signal line.

As per claim 18, Tamura et al inherently includes, wherein said equalization mechanism is configured to compensate for reflection of said signal over a signal line.

As per claim 19, Tamura et al inherently includes wherein said signal is transmitted over a first signal line and creates crosstalk in a second signal line, and said equalization mechanism is coupled between said first and second lines and configured to compensate for said crosstalk in said second line.

As per claim 21, Tamura et al inherently includes wherein said main drivers and equalization mechanism each include a current source, and said signal levels are voltages that are in a range between ground and a positive voltage.

As per claim 22, Tamura et al inherently includes, wherein said equalization mechanism further comprises a delay element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after delay by said delay element, and to output on said first line a fourth signal.

As per claim 23, Tamura et al inherently includes wherein said equalization mechanism further comprises an inversion element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after inversion by said inversion element, and to output on said first line a fourth signal.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimoto et al U.S. patent No 6,414,890 B2 teaches a semiconductor memory device.

Arcoleo et al U.S. Patent No 5,864,506 teaches a memory having selectable output.

Manning U.S. patent No 5,835,440 teaches a memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

4/20/05

EMMANUEL BAYARD
PRIMARY EXAMINER

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
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	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
EB	A	4,481,625	11/06/84	Roberts, et al	370	85	
	B	5,534,795	07/09/96	Wert, et al	326	81	
	C	5,534,798	07/09/96	Phillips, et al	326	108	
	D	5,663,663	09/02/97	Cao, et al	326	82	
	E	5,751,168	05/12/98	Speed, III et al	326	83	
	F	5,757,712	05/26/98	Nagel, et al	365	226	
	G	5,867,010	02/02/99	Hinedi, et al	323	282	
	H	5,973,508	10/26/99	Nowak, et al	326	81	
	I	5,986,472	11/16/99	Hinedi, et al	326	68	
	J	6,097,215	08/01/00	Bialas Jr., et al	326	68	
	K	6,140,841	10/31/00	Suh	326	60	
	L	6,160,421	12/12/00	Barna	326	63	
	M	4,748,637	05/31/88	Bishop, et al	375	7	
	N	5,254,883	10/19/93	Horowitz, et al	307	443	
	O	5,608,755	03/04/97	Rakib	375	219	
	P	5,546,042	08/13/96	Tedrow, et al	327	538	
	Q	5,194,765	03/16/93	Dunlop, et al	307	443	
EB	R	5,254,883	10/19/93	Horowitz, et al	307	443	

Examiner [signature] Date Considered 5/6/05

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U.S. Patent Documents

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KB	S	5,513,327	04/30/96	Farmwald, et al	395	309	
	T	5,023,488	06/11/91	Gunning	307	475	
	U	5,483,110	01/09/96	Koide, et al	307	147	
	V	5,287,108	02/15/94	Mayes, et al	341	156	
	W	5,977,798	11/02/99	Zerbe	329	98	
	X	RE30,182	12/25/79	Howson	325	42	
	Y	2,912,684	11/10/59	F.G. Steele	340	347	
	Z	3,051,901	08/28/62	R.E. Yaegar	325	38	
	AA	3,078,378	02/19/63	C.H. Burley, et al	307	88.5	
	AB	3,267,459	08/16/66	J.S. Chomicki, et al	340	347	
	AC	3,484,559	12/16/69	D.F. Rigby	179	18	
	AD	3,508,076	04/21/70	R.O. Winder	307	235	
	AE	3,510,585	05/05/70	R.B. Stone	325	38	
	AF	3,560,856	02/02/71	Hisashi, Kaneko	375	292	
	AG	3,569,955	03/09/71	Maniere	340	347	
	AH	3,571,725	03/23/71	Kaneko, et al	328	14	
	AI	3,587,088	06/22/71	Franaszek	340	347	
KB	AJ	3,648,064	03/07/72	Mukai, et al	307	213	

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EB	AK	3,697,874	10/10/72	Kaneko	325	38 A	
	AL	3,731,199	05/01/73	Tazaki, et al	325	38 A	
	AM	3,733,550	05/15/73	Tazaki, et al	325	38 A	
	AN	3,753,113	08/14/73	Maruta, et al	325	38 A	
	AO	3,754,237	08/21/73	de Laage de Meux	340	347 DD	
	AP	3,761,818	09/25/73	Tazaki, et al	325	38 A	
	AQ	3,772,680	11/13/73	Kawai, et al	340	347 DD	
	AR	3,798,544	03/19/74	Norman	325	38 A	
	AS	3,832,490	08/27/74	Leonard	178	68	
	AT	3,860,871	01/14/75	Hinoshita, et al	325	38 B	
	AU	3,876,944	04/08/75	Mack, et al	325	141	
	AV	3,927,401	12/16/75	McIntosh	340	347 DD	
	AW	3,978,284	08/31/76	Yoshino, et al	178	69.5 R	
	AX	3,988,676	10/26/76	Whang	325	38 A	
	AY	4,038,564	07/26/77	Hakata	307	205	
	AZ	4,070,650	01/24/78	Ohashi, et al	340	172	
	BA	4,086,587	04/25/78	Lender	340	347 DD	
EB	BB	4,097,859	06/27/78	Looschen	340	347 DD	

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EB	BC	4,131,761	12/26/78	Giusto	179	15 BY	
	BD	4,181,865	01/01/80	Kohyama	307	361	
	BE	4,373,152	02/08/83	Jacobsthal	340	347	
	BF	4,382,249	05/03/83	Jacobsthal	340	347 DD	
	BG	4,403,330	09/06/83	Meyer	375	4	
	BH	4,408,135	10/04/83	Yuyama, et al	307	474	
	BI	4,408,189	10/04/83	Betts, et al	340	347 DD	
	BJ	4,528,550	07/09/85	Graves, et al	340	347 DD	
	BK	4,438,491	03/20/84	Constant	364	200	
	BL	4,571,735	02/18/86	Furse	375	20	
	BM	4,602,374	07/22/86	Nakamura, et al	375	17	
	BN	4,628,297	12/09/86	Mita, et al	340	347 DD	
	BO	4,779,073	10/18/88	Iketani	341	55	
	BP	4,805,190	02/14/89	Jaffre, et al	375	17	
	BQ	4,821,286	04/11/89	Graczyk, et al	375	4	
	BR	4,823,028	04/18/89	Lloyd	307	355	
	BS	4,841,301	06/20/89	Ichihara	341	126	
EB	BT	4,860,309	08/22/89	Costello	375	17	

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EB	BU	4,875,049	10/17/89	Yoshida	341	159	
	BV	4,888,764	12/19/89	Haug	370	85.1	
	BW	5,003,555	03/26/91	Bergmans	375	12	
	BX	5,045,728	09/03/91	Crafts	307	475	
	BY	5,115,450	05/19/92	Arcuri	375	7	
	BZ	5,121,411	06/09/92	Fluharty	375	20	
	CA	5,172,338	12/15/92	Mehrotra, et al	365	185	
	CB	5,191,330	03/02/93	Fisher, et al	341	56	
	CC	5,230,008	07/20/93	Duch, et al	375	19	
	CD	5,243,625	09/07/93	Verbakel, et al	375	17	
	CE	5,280,500	01/18/94	Mazzola, et al	375	17	
	CF	5,295,155	03/15/94	Gersbach, et al	375	4	
	CG	5,315,175	05/24/94	Langner	307	443	
	CH	5,331,320	07/19/94	Cideciyan, et al	341	56	
	CI	5,408,498	04/18/95	Yoshida	375	286	
	CJ	5,425,056	06/13/95	Maroun, et al	375	316	
	CK	5,426,739	06/20/95	Lin, et al	395	325	
EB	CL	5,438,593	08/01/95	Karam, et al	375	317	

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a-h	CM	5,459,749	10/17/95	Park	375	286	
	CN	5,471,156	11/28/95	Kim, et al	326	60	
	CO	5,473,635	12/05/95	Chevroulet	375	287	
	CP	5,525,983	06/11/96	Patel, et al	341	57	
	CQ	5,663,631	09/02/97	Kajiura, et al	322	29	
	CR	5,640,605	06/17/97	Johnson, et al	395	881	
	CS	5,684,833	11/04/97	Watanabe	375	286	
	CT	5,740,201	04/14/98	Hui	375	286	
	CU	5,793,815	08/11/98	Goodnow, et al	375	286	
	CV	5,793,816	08/11/98	Hui	375	286	
	CW	5,796,781	08/18/98	DeAndrea, et al	375	288	
	CX	5,825,825	10/20/98	Altmann, et al	375	293	
	CY	5,872,468	02/16/99	Dyke	327	72	
	CZ	5,892,466	04/06/99	Walker	341	57	
	DA	5,898,734	04/27/99	Nakamura, et al	375	287	
	DB	5,917,340	06/29/99	Manohar, et al	326	82	
	DC	5,933,458	08/03/99	Leurent, et al	375	317	
a-h	DD	5,942,994	08/24/99	Lewiner, et al	341	56	

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✓	DE	5,946,355	08/31/99	Baker	375	286	
	DF	5,949,280	09/07/99	Sasaki	329	303	
	DG	5,969,579	10/19/99	Hartke, et al	332	116	
	DH	5,969,648	10/19/99	Garnett	341	56	
	DI	6,018,550	01/25/00	Emma, et al	375	317	
	DJ	6,038,260	03/14/00	Emma, et al	375	259	
	DK	6,049,229	04/11/00	Manohar, et al	326	83	
	DL	6,052,390	04/18/00	Deliot, et al	370	258	
	DM	6,067,326	05/23/00	Jonsson, et al	375	286	
	DN	6,078,627	06/20/00	Crayford	375	286	
	DO	6,048,931	04/11/00	Fujita, et al	525	67	
	DP	6,094,461	07/25/00	Heron	375	317	
	DQ	6,101,561	08/08/00	Beers, et al	710	66	
	DR	6,114,979	09/05/00	Kim	341	57	
	DS	6,122,010	09/19/00	Emelko	348	461	
	DT	6,140,841	10/31/00	Suh	326	60	
✓	DU	6,195,397	02/27/01	Kwon	375	288	
✓	DV	5,023,841	06/11/91	Akrout, et al	365	205	

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	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

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U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
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							Translation	
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	Attorney Docket No.: RA-194

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	Attorney Docket No.: RA-194

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U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
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"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

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U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/2000
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventors: Pak Shing Chau, et al.
	Group Art Unit: Unknown
"LOW-LATENCY EQUILIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS"	Examiner Name: Unknown
	Attorney Docket No.: RA-194

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	B						
	C						
	D						
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							Translation	
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	9/22/04

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	Examiner Emmanuel Bayard	Art Unit 2631	Page 1 of 1

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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

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Examiner Signature		Date Considered	5/10/05

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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